

FIG. 1

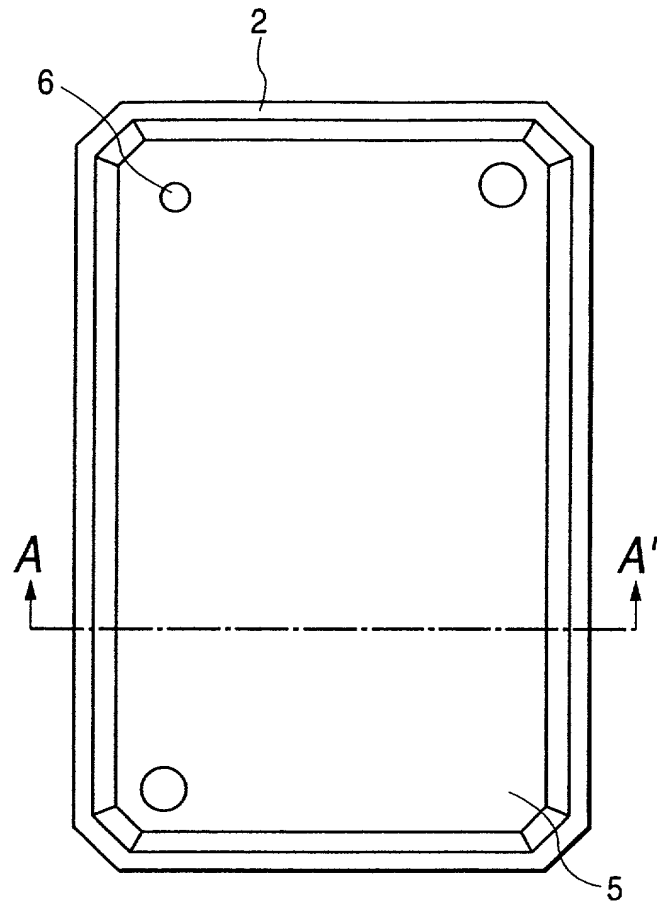


FIG. 3

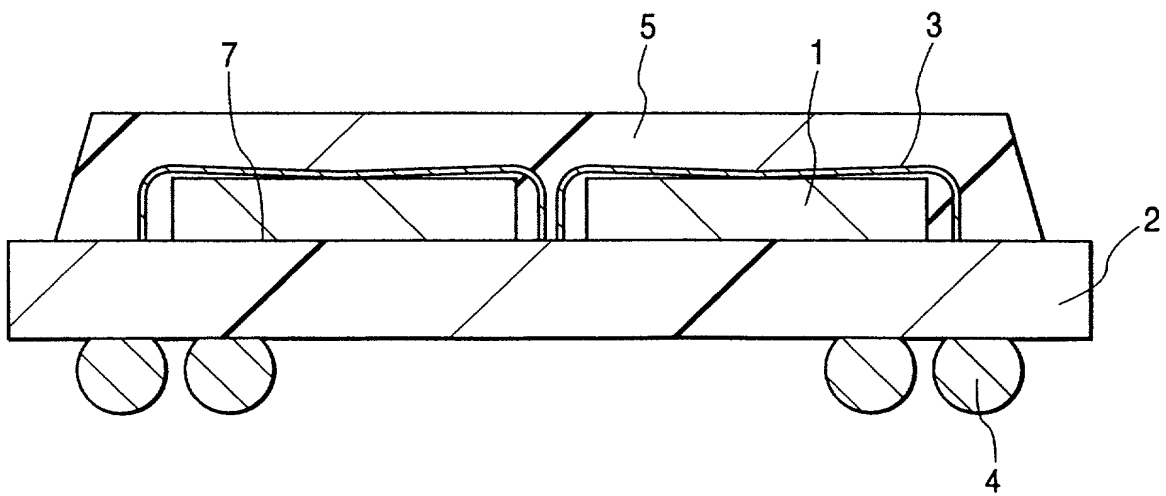


FIG. 2(a)

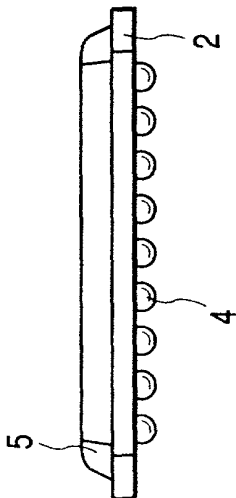


FIG. 2(b)

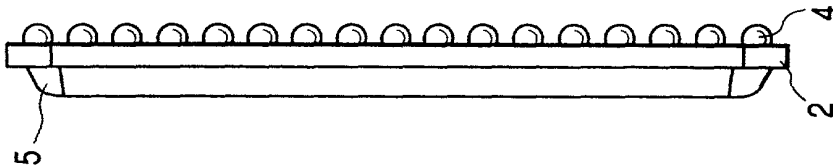


FIG. 2(c)

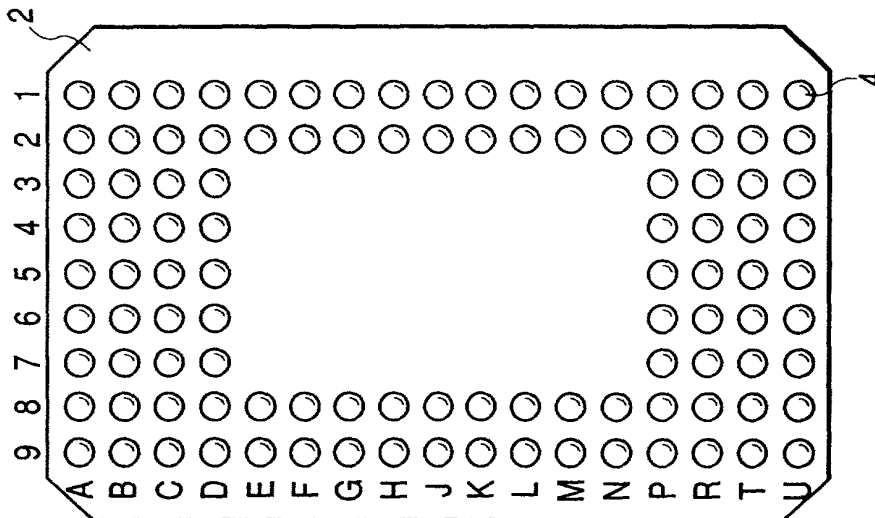


FIG. 4

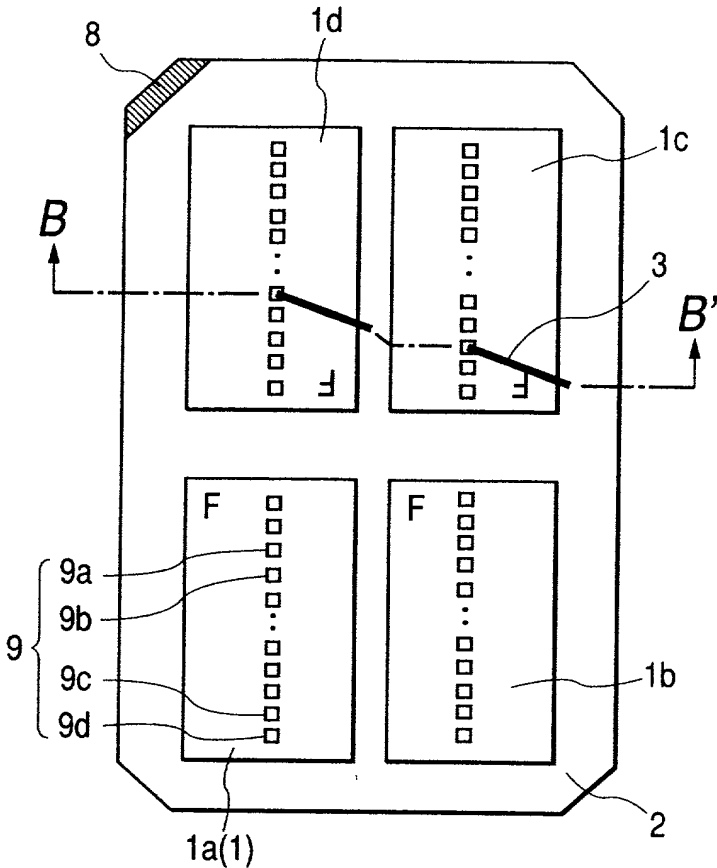


FIG. 5

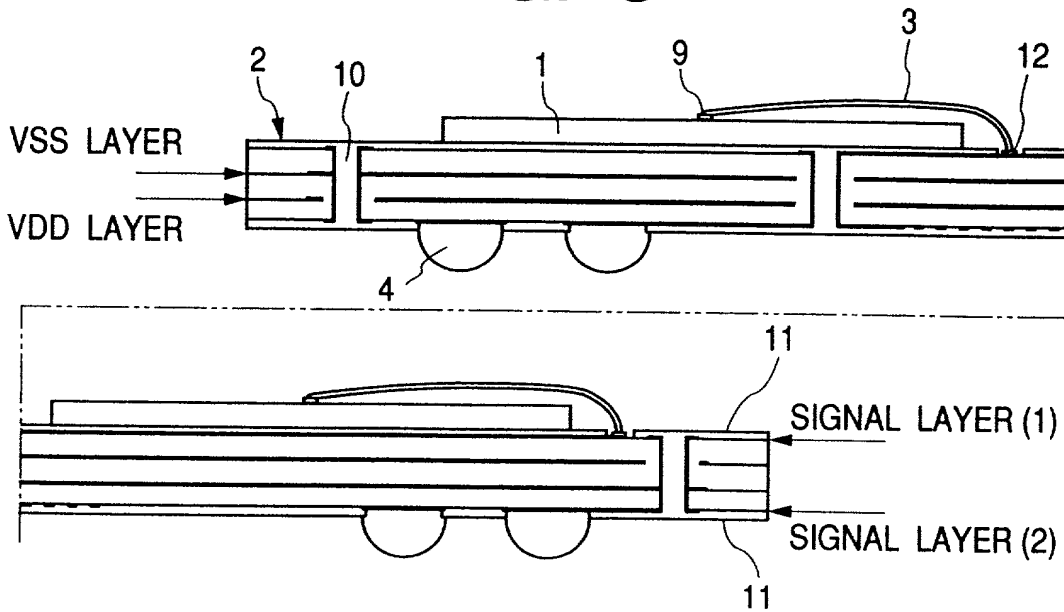
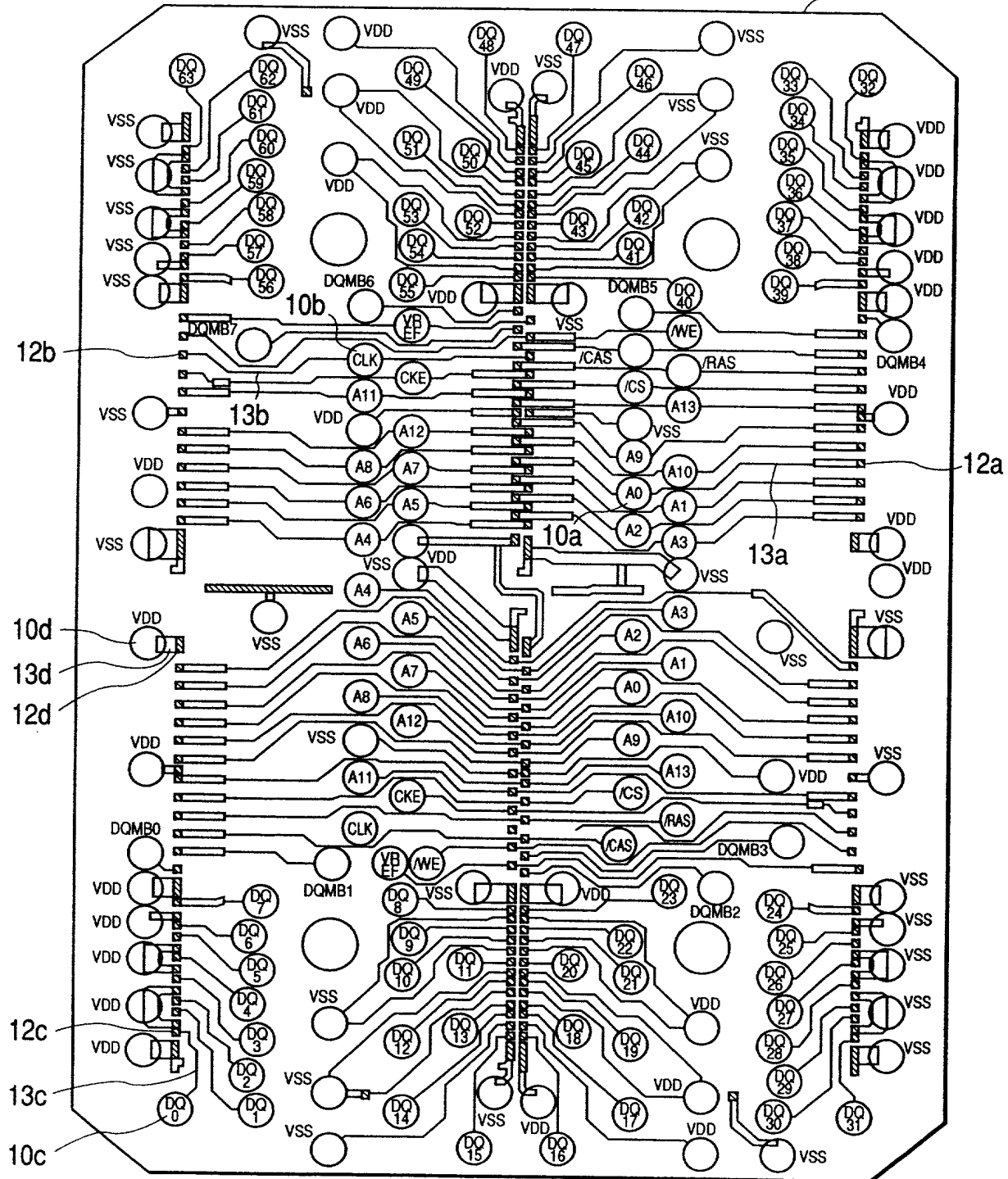


FIG. 6

2 (1ST LAYER)



□ : PADS (12) ○ : THROUGH-HOLES (10) ○ : PENETRATION HOLDS (15)

FIG. 7

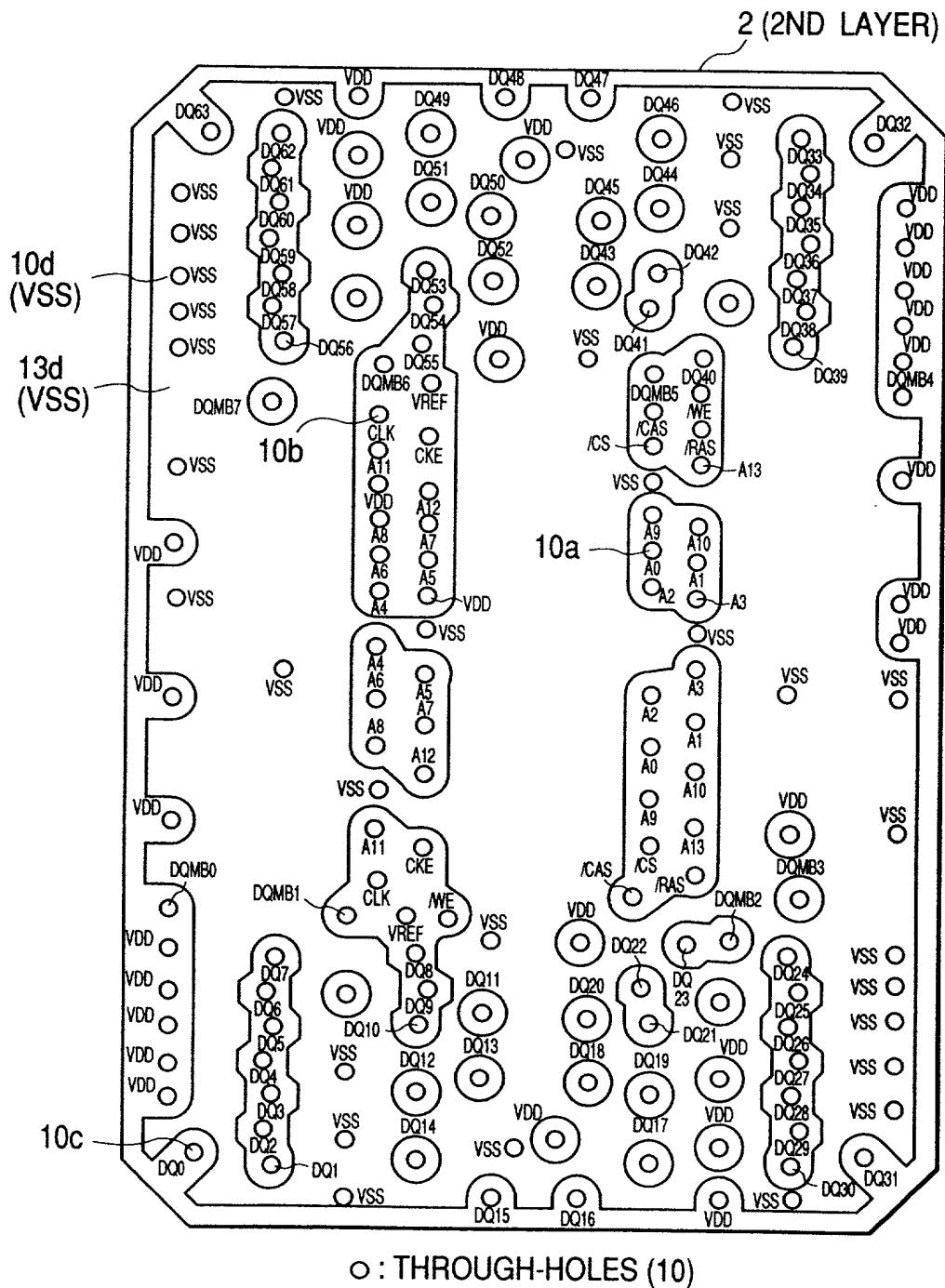


FIG. 8

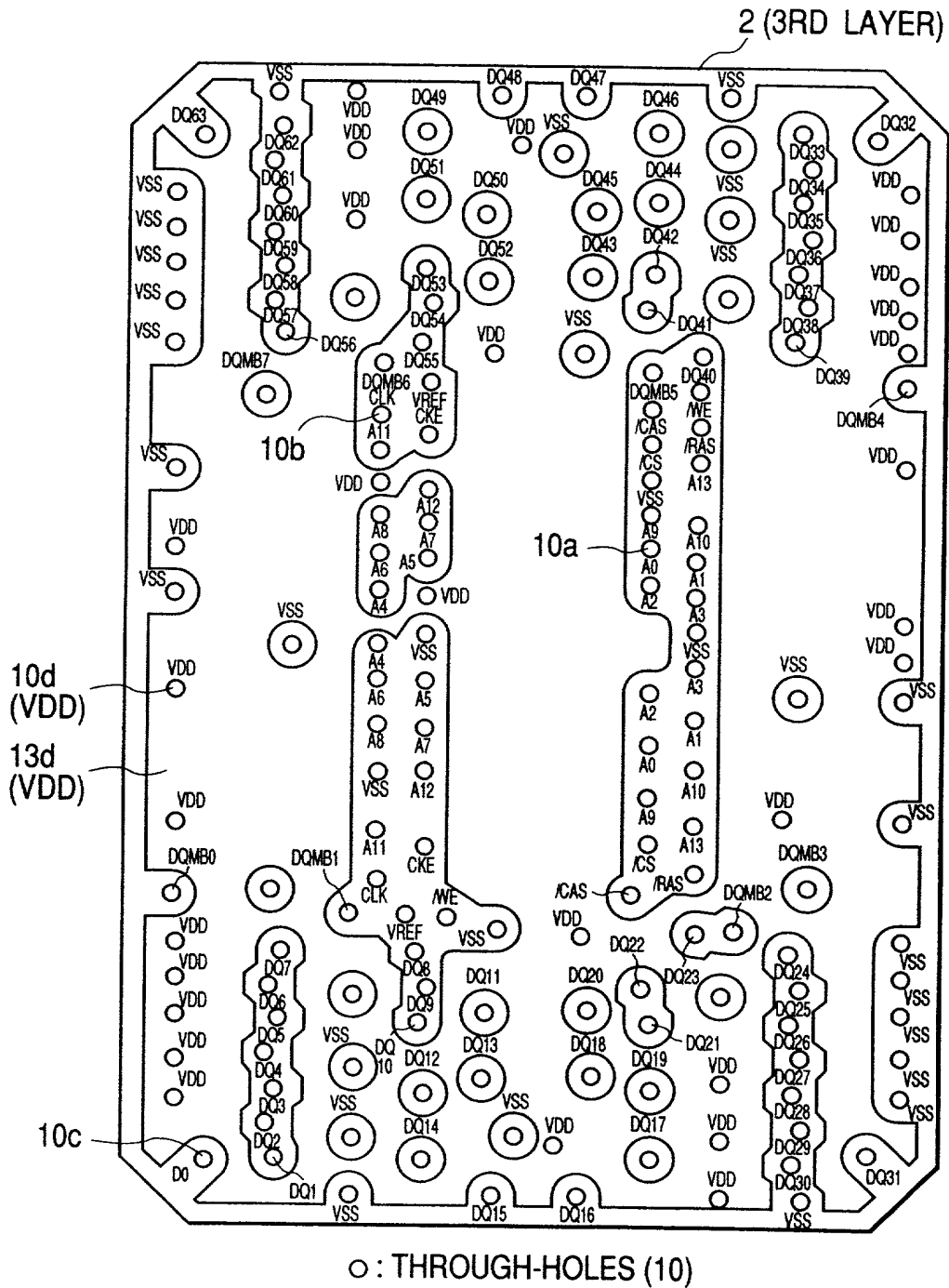


FIG. 9

2 (4TH LAYER)

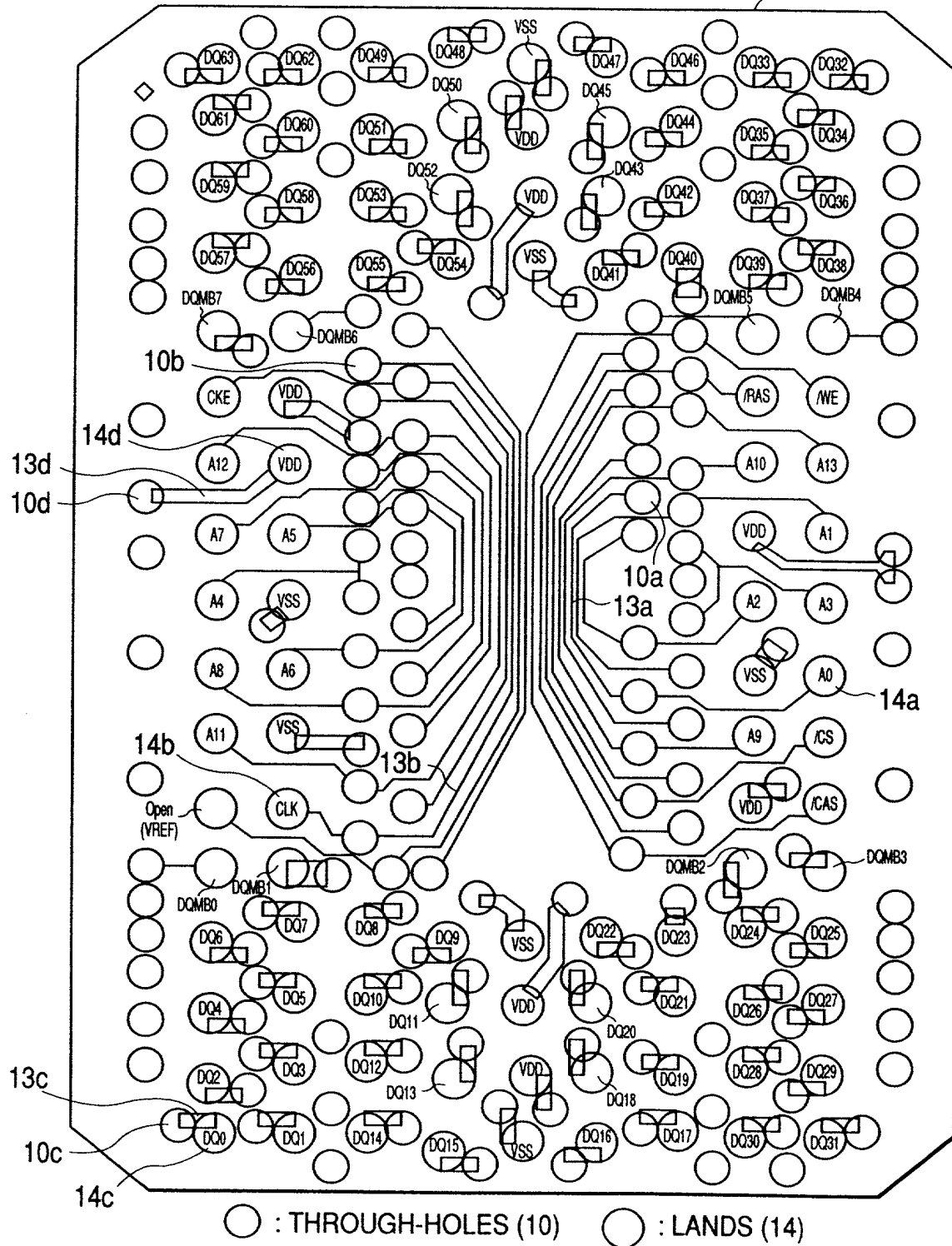


FIG. 10

2 (1ST & 4TH LAYERS)

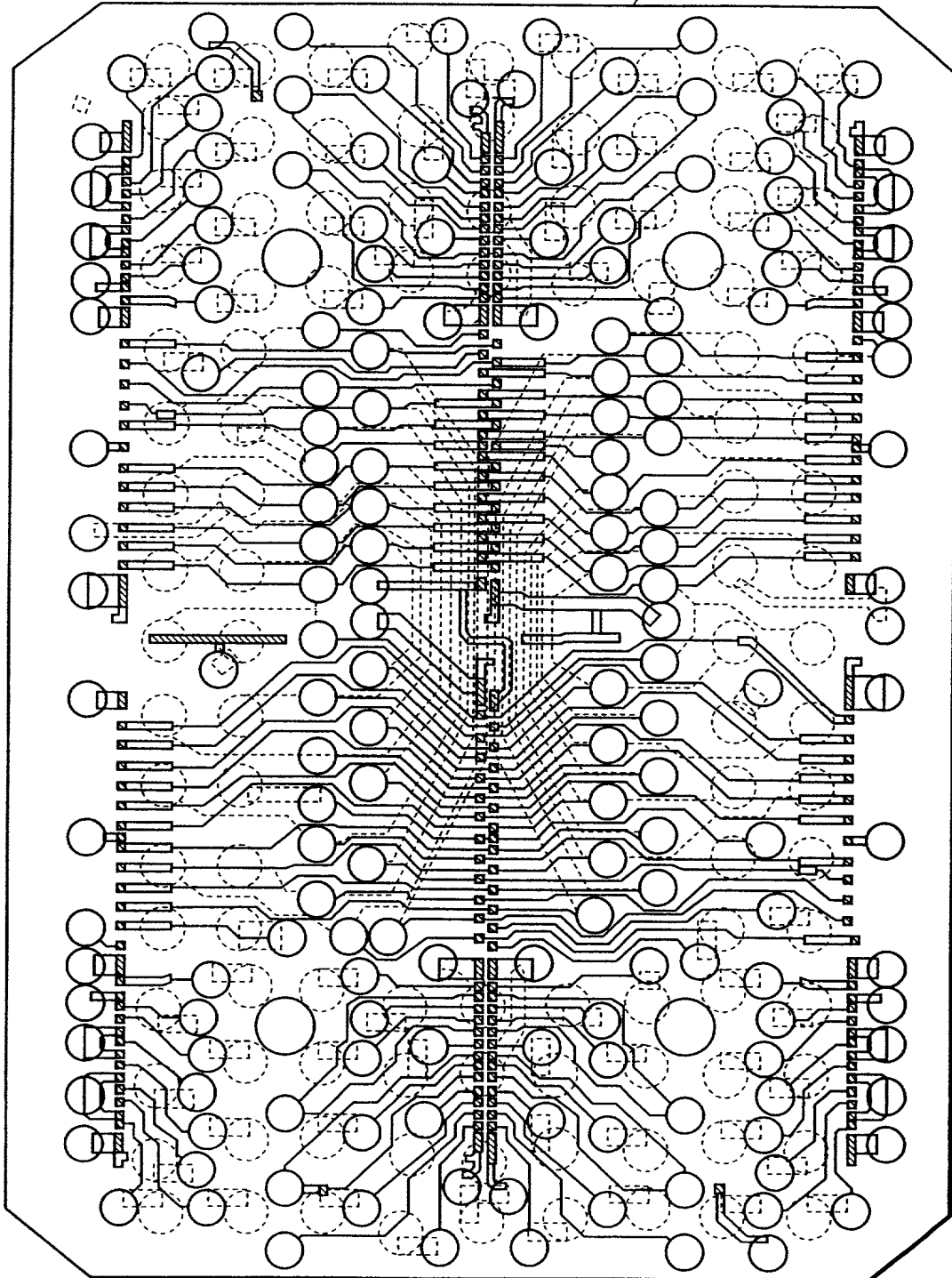


FIG. 11

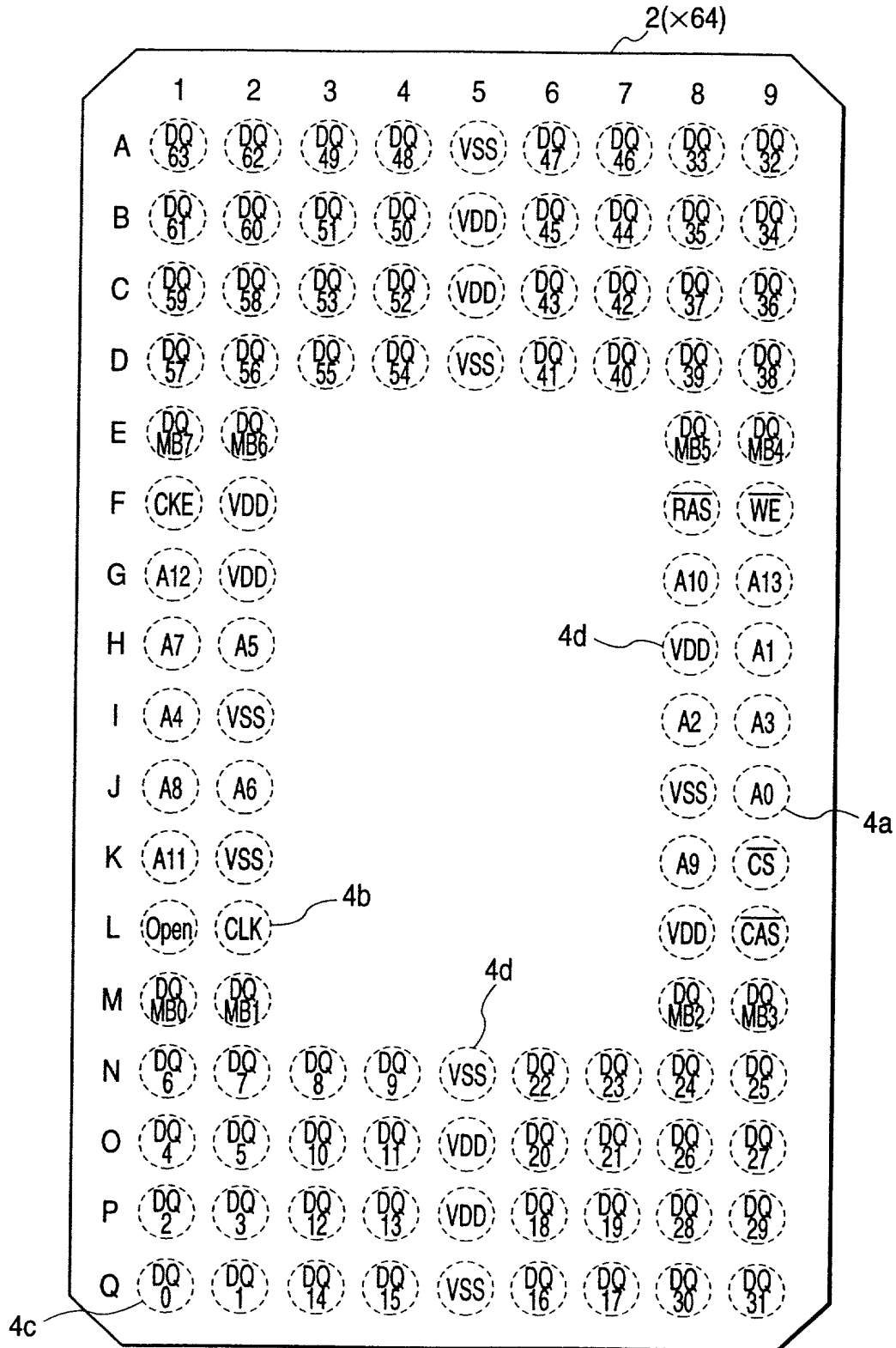


FIG. 12

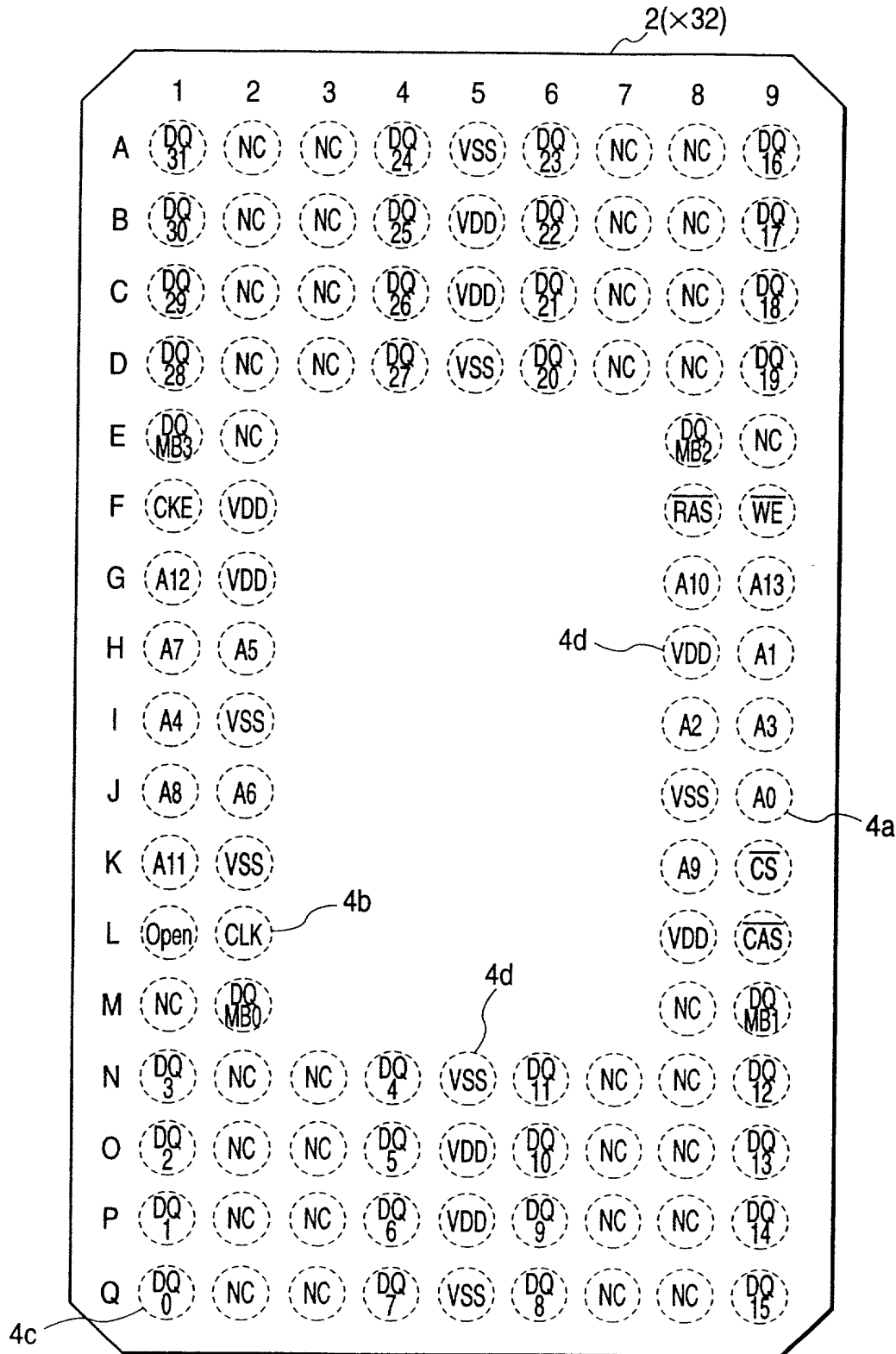
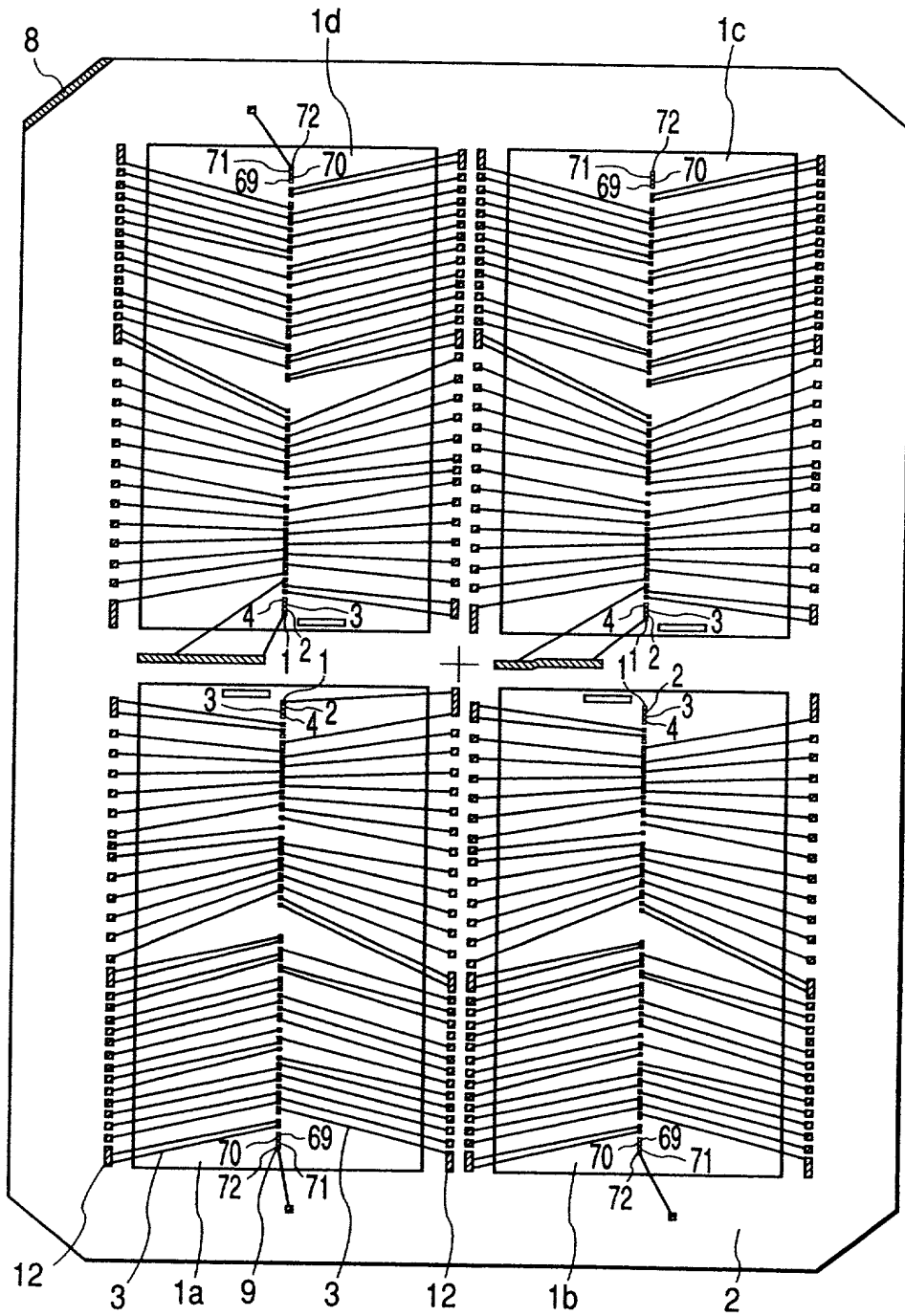


FIG. 13



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FIG. 14

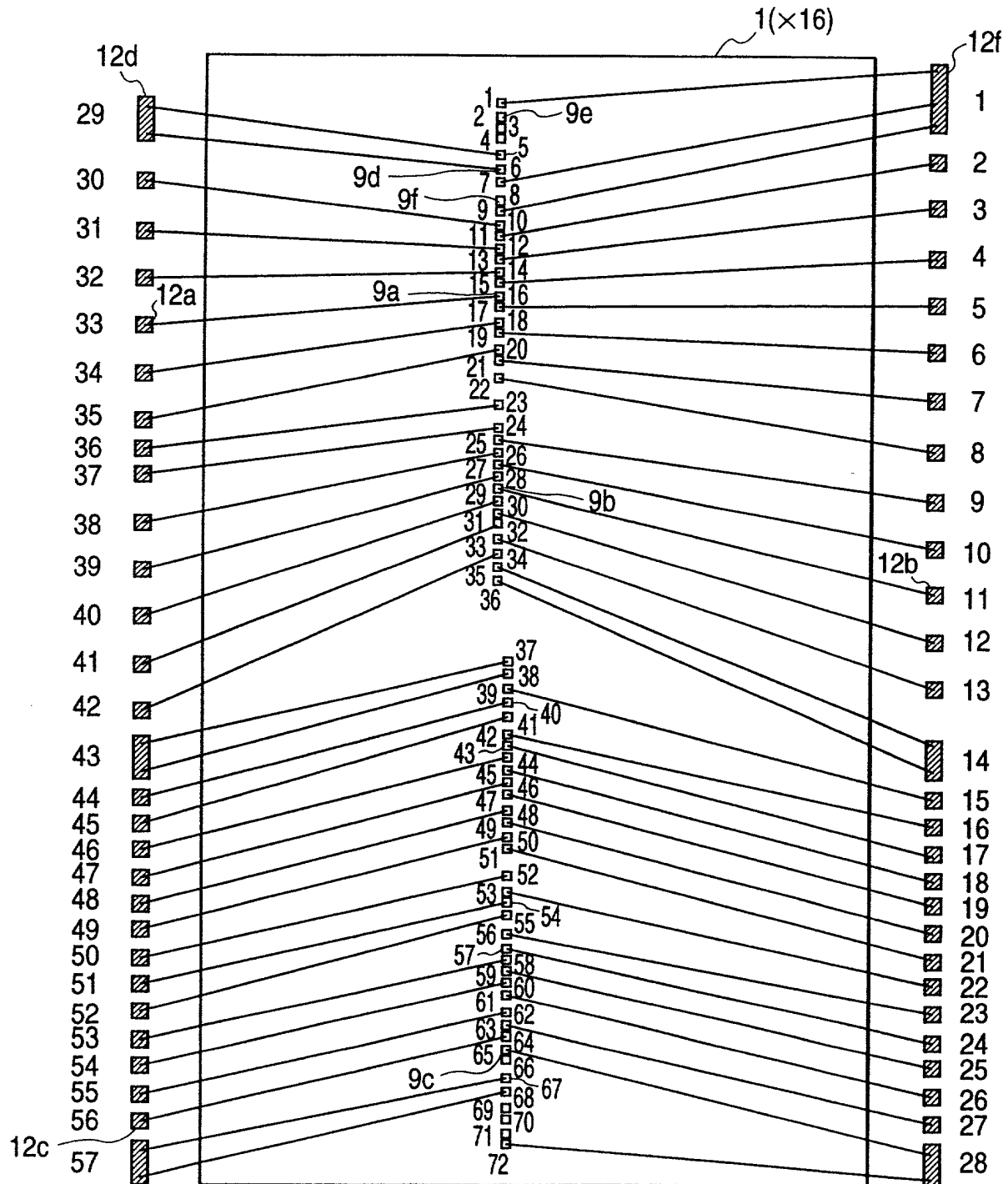


FIG. 15

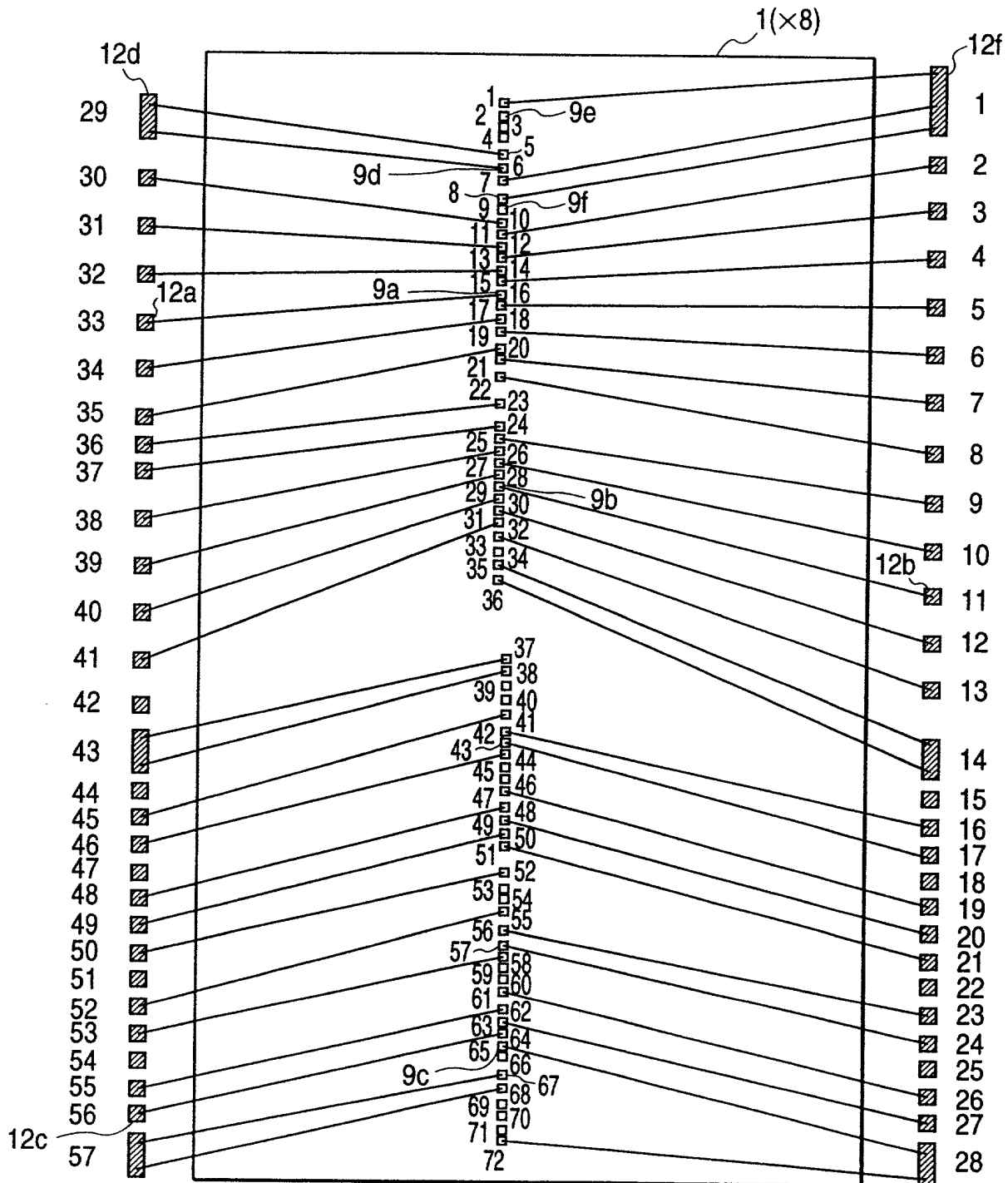


FIG. 16

PAD NO.	PAD NAMES	USE
1	VSSI	POWER SUPPLY
2	VBB	P-TEST
3	VPLT	P-TEST
4	VPP	P-TEST
5	VDDI	POWER SUPPLY
6	VDD	POWER SUPPLY
7	VSS	POWER SUPPLY
8	BOP1B	BONDING OPTION
9	BOP2B	BONDING OPTION
10	A3	INPUT (ADDRESS)
11	A4	INPUT (ADDRESS)
12	A2	INPUT (ADDRESS)
13	A5	INPUT (ADDRESS)
14	A1	INPUT (ADDRESS)
15	A6	INPUT (ADDRESS)
16	A0	INPUT (ADDRESS)
17	A7	INPUT (ADDRESS)
18	A10	INPUT (ADDRESS)
19	A8	INPUT (ADDRESS)
20	A12	INPUT (ADDRESS)
21	A9	INPUT (ADDRESS)
22	VSS	POWER SUPPLY
23	VDD	POWER SUPPLY
24	A13	INPUT (ADDRESS)
25	A11	INPUT (ADDRESS)
26	/CS	INPUT (CONTROL)
27	CKE	INPUT (CONTROL)
28	/RAS	INPUT (CONTROL)
29	CLK	INPUT (CONTROL)
30	/CAS	INPUT (CONTROL)
31	DQMU	INPUT (CONTROL)
32	/WE	INPUT (CONTROL)
33	VREF	INPUT (CONTROL)
34	DQML	INPUT (CONTROL)
35	VSSI	POWER SUPPLY
36	VSS	POWER SUPPLY
CHIP CENTER		

PAD NO.	PAD NAMES	USE
37	VDD	POWER SUPPLY
38	VDDI	POWER SUPPLY
39	DQ8	I/O DATA
40	DQ7	I/O DATA
41	VDDQ	POWER SUPPLY
42	VSSQ	POWER SUPPLY
43	DQ9	I/O DATA
44	DQ6	I/O DATA
45	DQ10	I/O DATA
46	DQ5	I/O DATA
47	VSSQ	POWER SUPPLY
48	VDDQ	POWER SUPPLY
49	DQ11	I/O DATA
50	DQ4	I/O DATA
51	VSS	POWER SUPPLY
52	VDD	POWER SUPPLY
53	DQ12	I/O DATA
54	DQ3	I/O DATA
55	VDDQ	POWER SUPPLY
56	VSSQ	POWER SUPPLY
57	DQ13	I/O DATA
58	DQ2	I/O DATA
59	DQ14	I/O DATA
60	DQ1	I/O DATA
61	VSSQ	POWER SUPPLY
62	VDDQ	POWER SUPPLY
63	DQ15	I/O DATA
64	DQ0	I/O DATA
65	VSS	POWER SUPPLY
66	BOP0B	BONDING OPTION
67	VDD	POWER SUPPLY
68	VDDIU	POWER SUPPLY
69	VPERI	P-TEST
70	VDL	P-TEST
71	VLBR	P-TEST
72	VSSIU	POWER SUPPLY
CHIP CENTER		

FIG. 17

SUBSTRATE	CHIP	
PAD NO.	PAD NAMES	
	×16	×8
1	VSS	VSS
	VSS	VSS
	BOP2B	—
	—	BOP1B
2	A4	A4
3	A5	A5
4	A6	A6
5	A7	A7
6	A8	A8
7	A12	A12
8	VSS	VSS
9	A11	A11
10	CKE	CKE
11	CLK	CLK
12	/WE	/WE
13	VREF	VREF
14	VSS	VSS
	VSS	VSS
15	DQ8	—
16	VSS	VSS
17	DQ9	DQ4
18	DQ10	—
19	VSS	VSS
20	DQ11	DQ5
21	VSS	VSS
22	DQ12	—
23	VSS	VSS
24	DQ13	DQ6
25	DQ14	—
26	VSS	VSS
27	DQ15	DQ7
28	VSS	VSS
	VSS	VSS

SUBSTRATE	CHIP	
PAD NO.	PAD NAMES	
	×16	×8
29	VDD	VDD
	VDD	VDD
30	A3	A3
31	A2	A2
32	A1	A1
33	A0	A0
34	A10	A10
35	A9	A9
36	VDD	VDD
37	A13	A13
38	/CS	/CS
39	/RAS	/RAS
40	/CAS	/CAS
41	DQMU	DQM
42	DQML	—
43	VDD	VDD
	VDD	VDD
44	DQ7	—
45	VDD	VDD
46	DQ6	DQ3
47	DQ5	—
48	VDD	VDD
49	DQ4	DQ2
50	VDD	VDD
51	DQ3	—
52	VDD	VDD
53	DQ2	DQ1
54	DQ1	—
55	VDD	VDD
56	DQ0	DQ0
57	VDD	VDD
	VDD	VDD

— : NC

FIG. 18

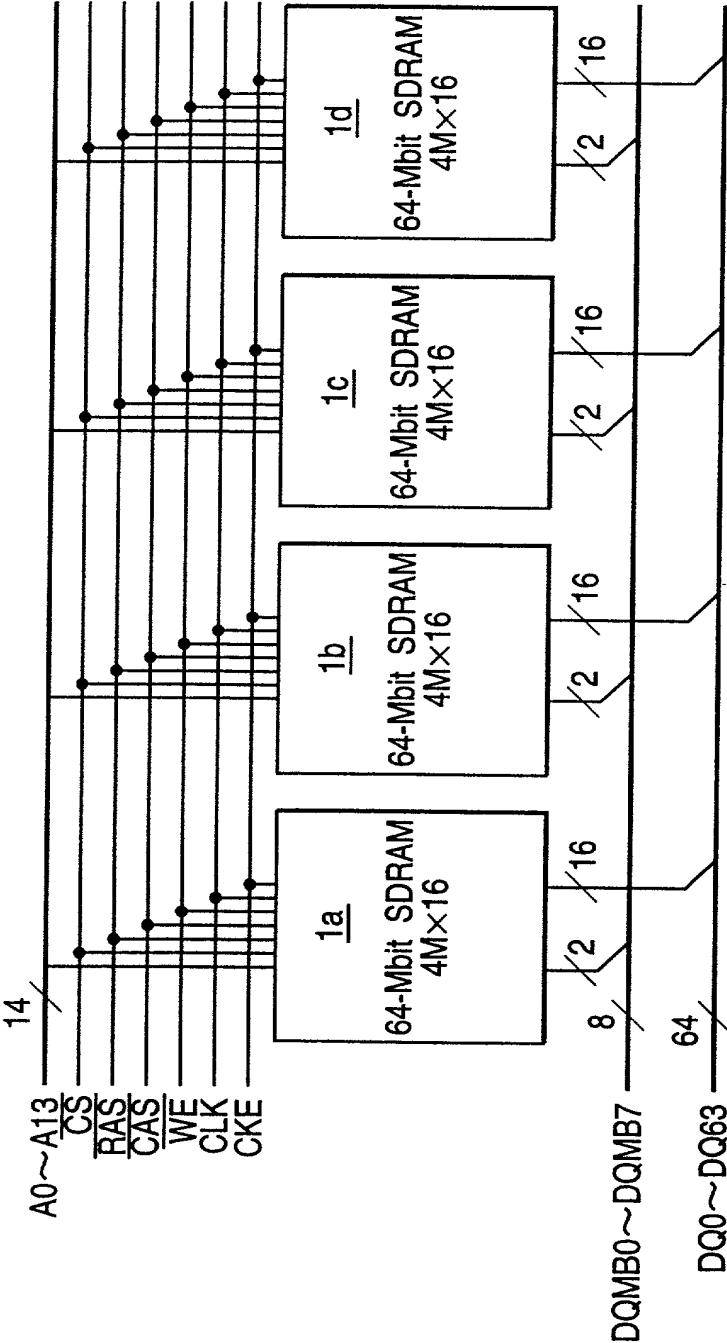


FIG. 19

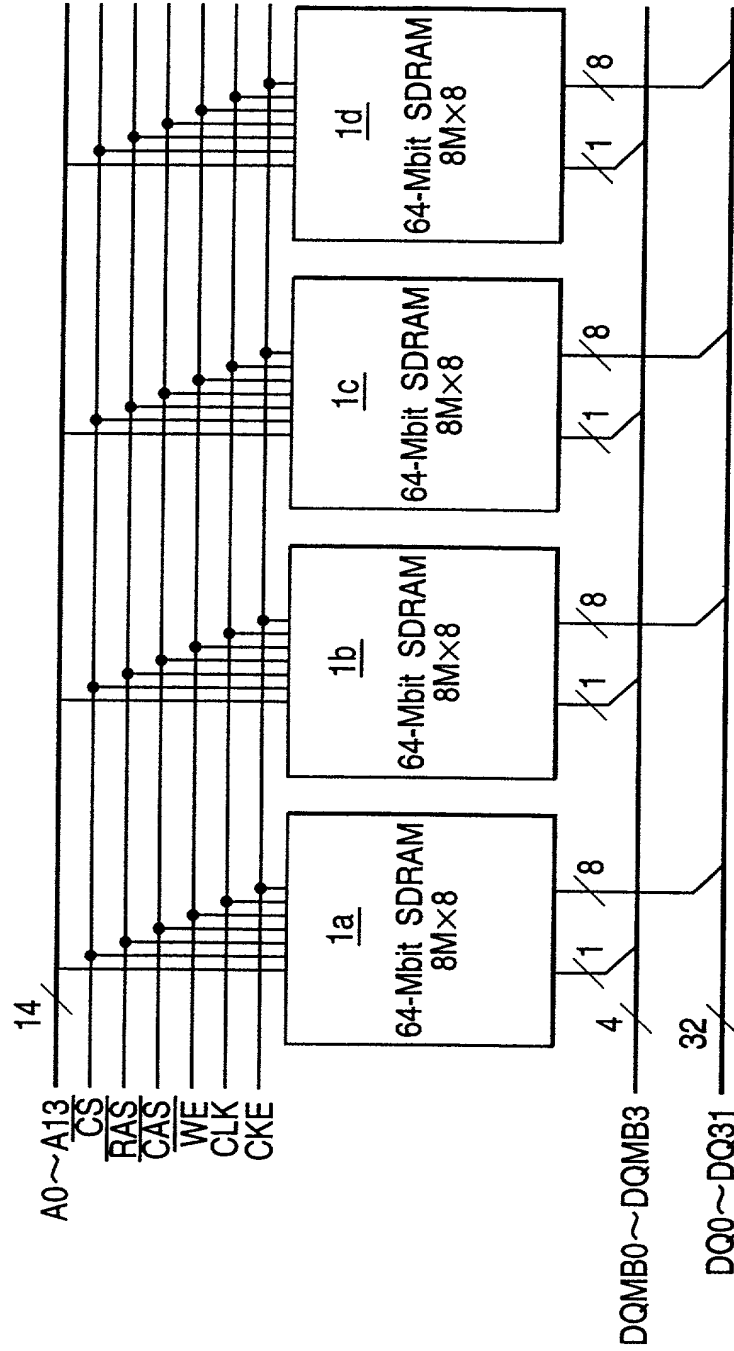


FIG. 20

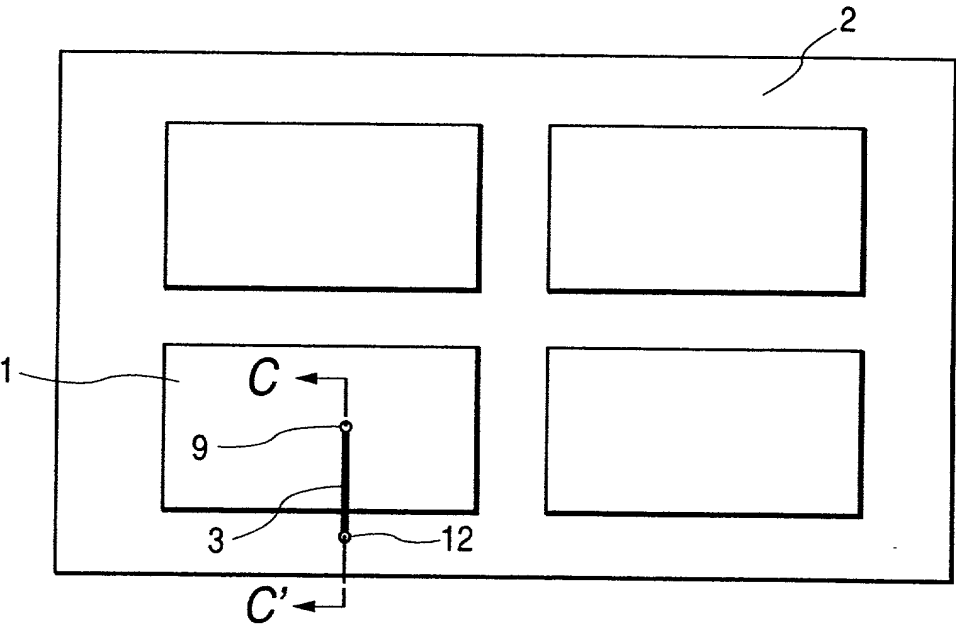


FIG. 21

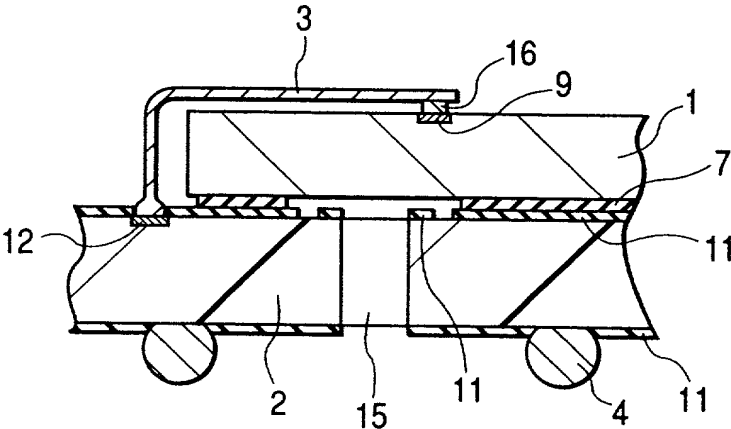
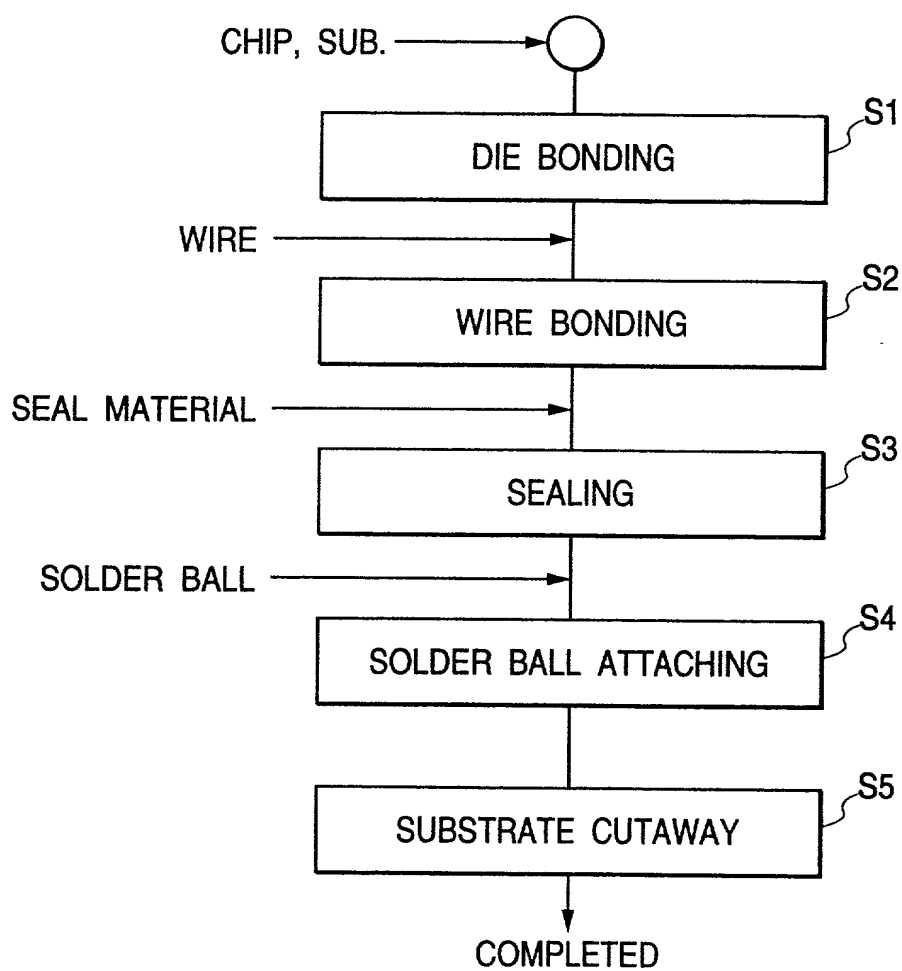


FIG. 22

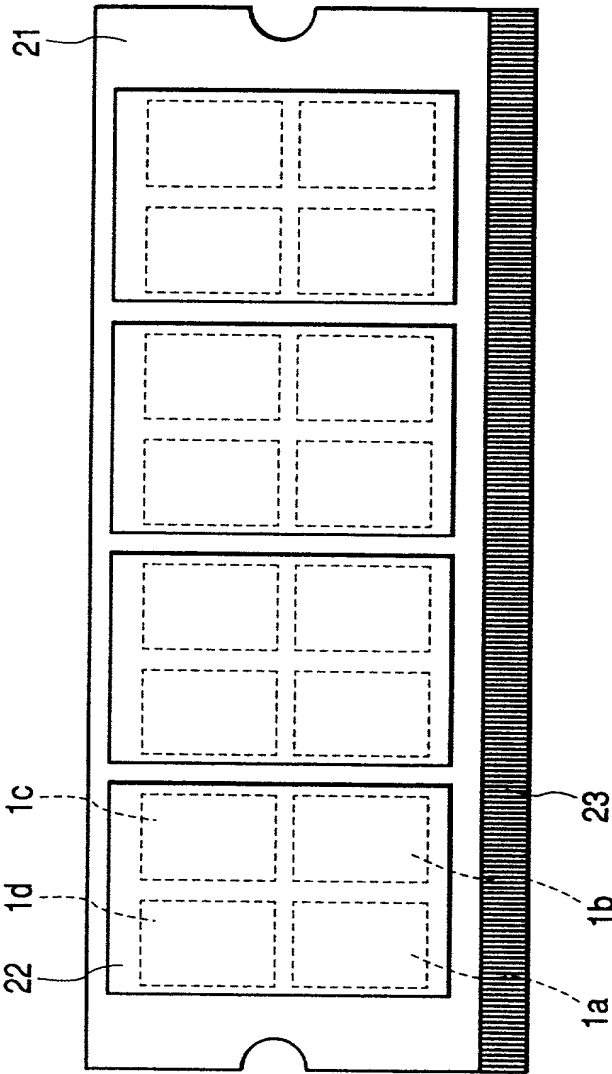


FIG. 23

FIG. 24

FIG. 24

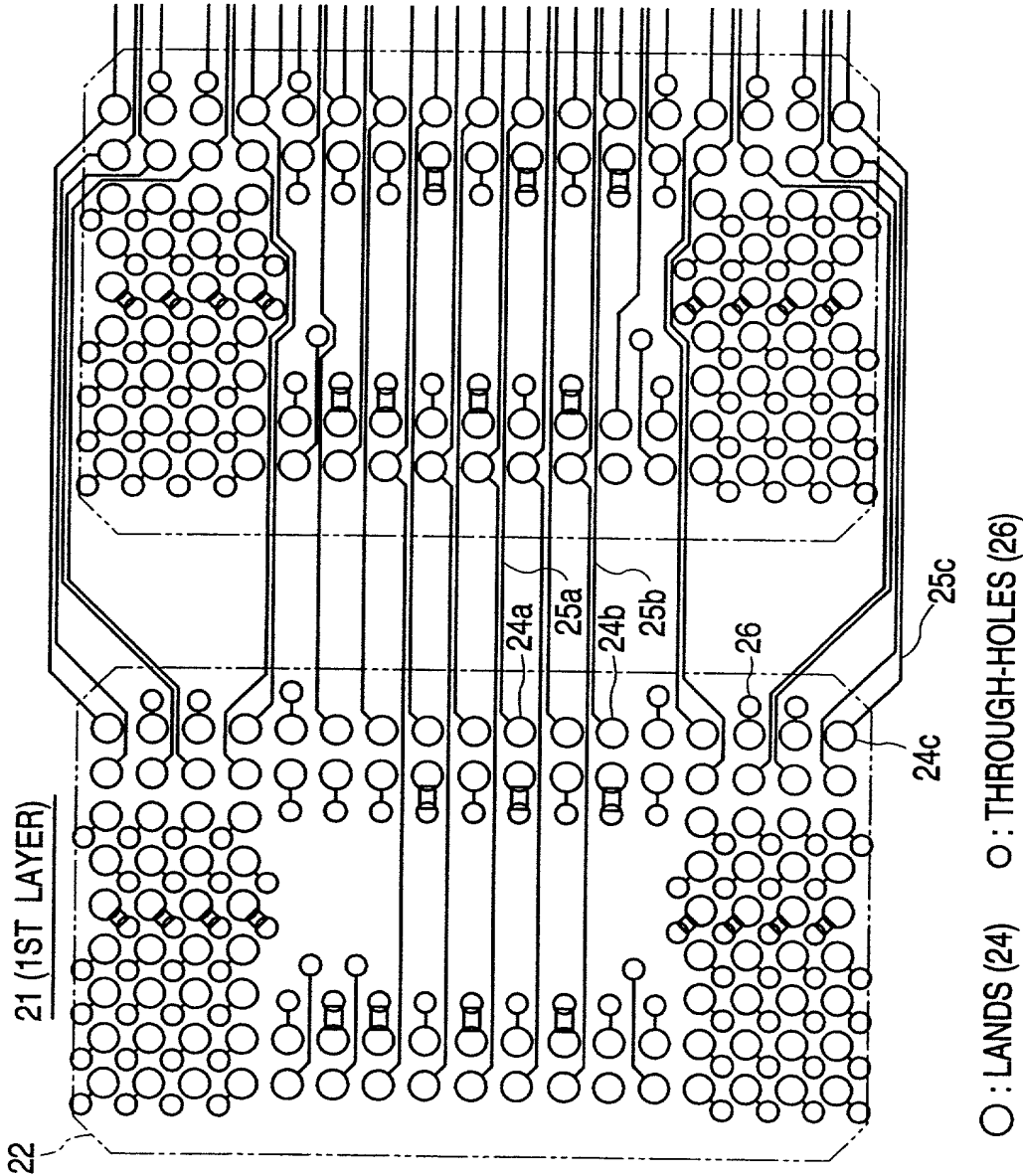


FIG. 25

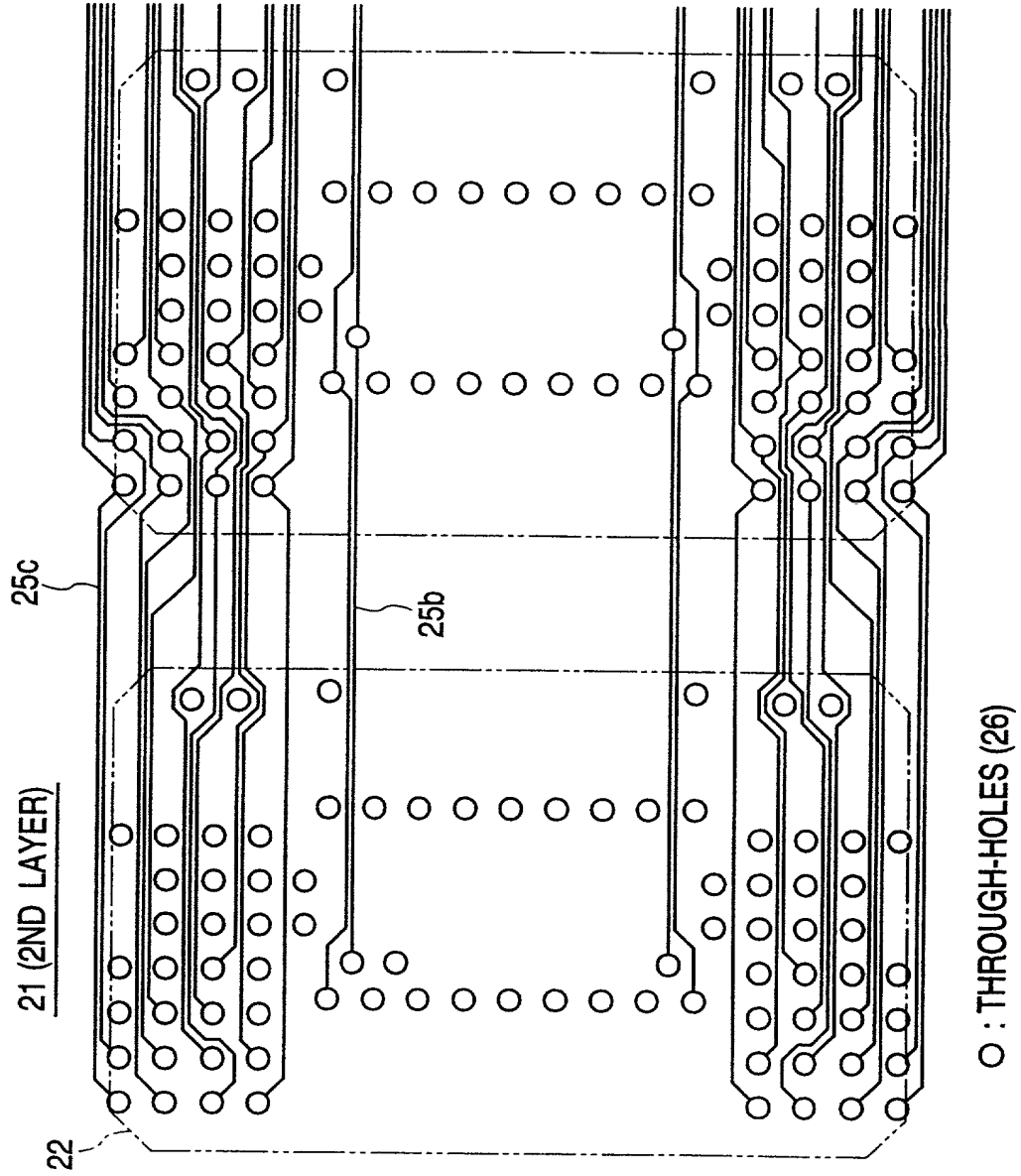


FIG. 26

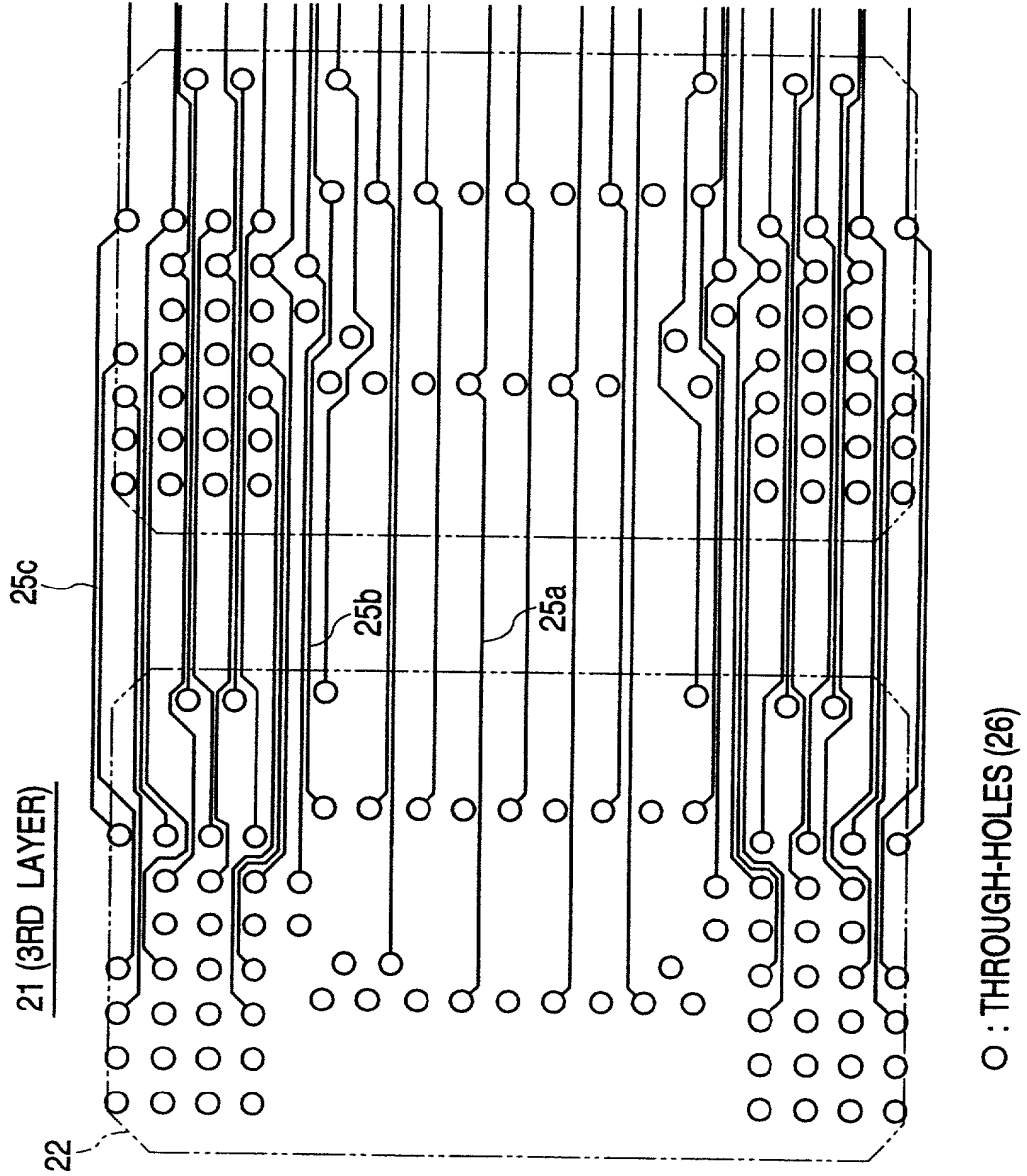


FIG. 27

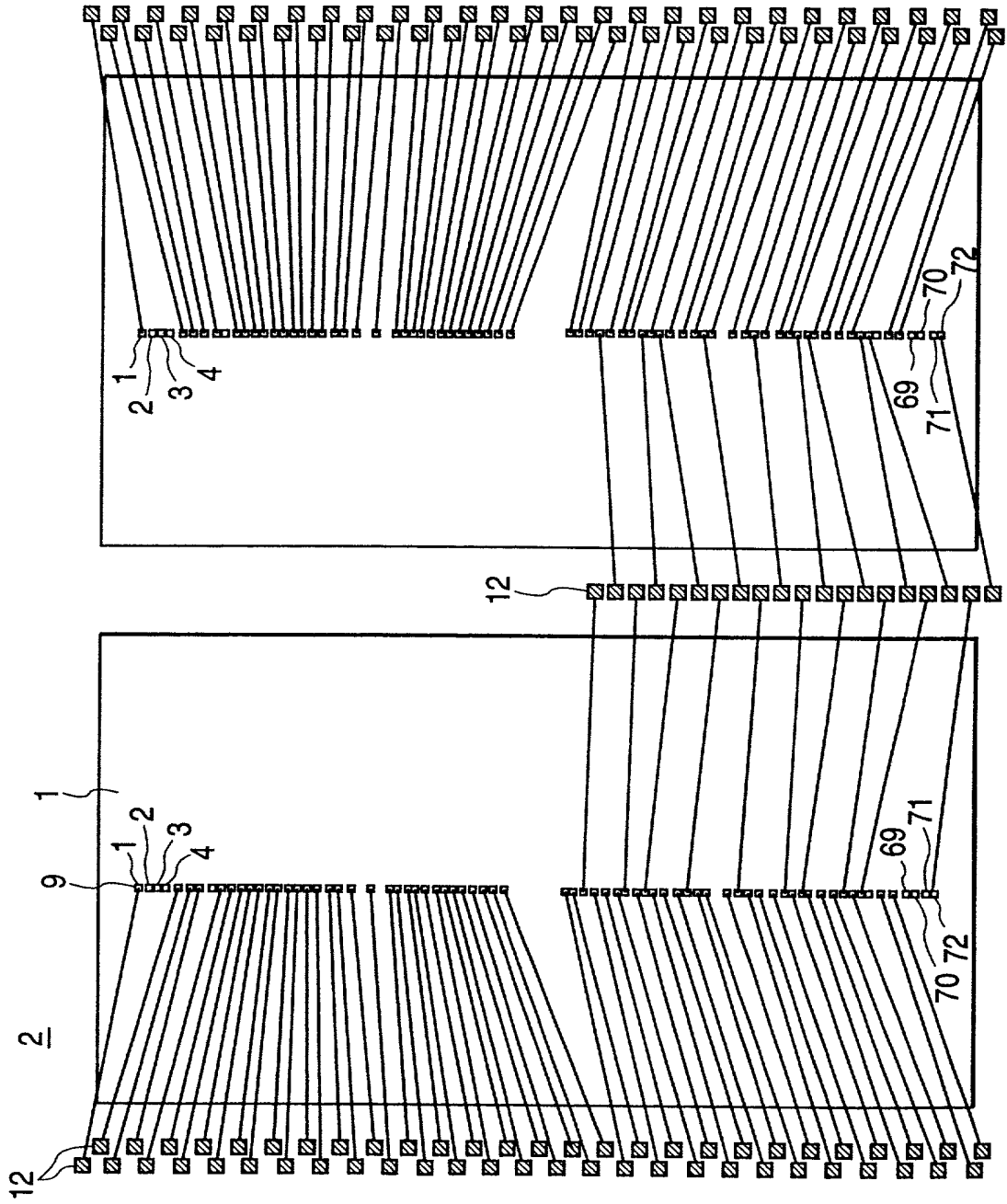


FIG. 28

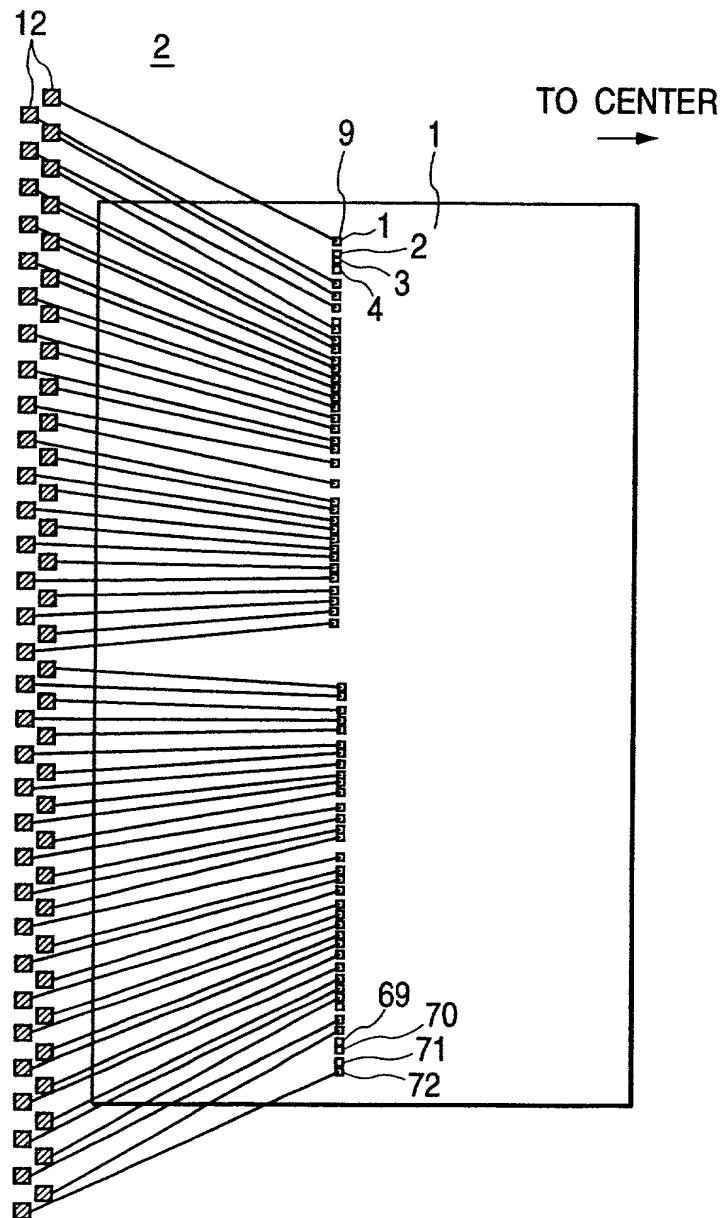


FIG. 29

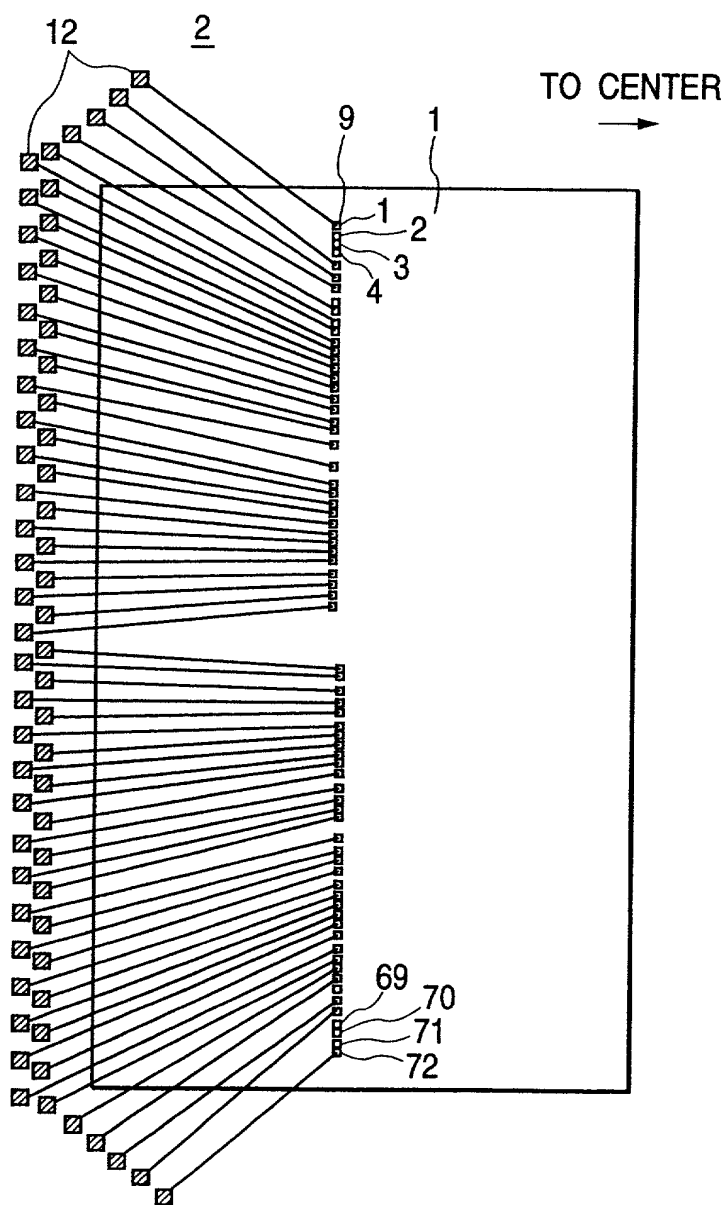


FIG. 30

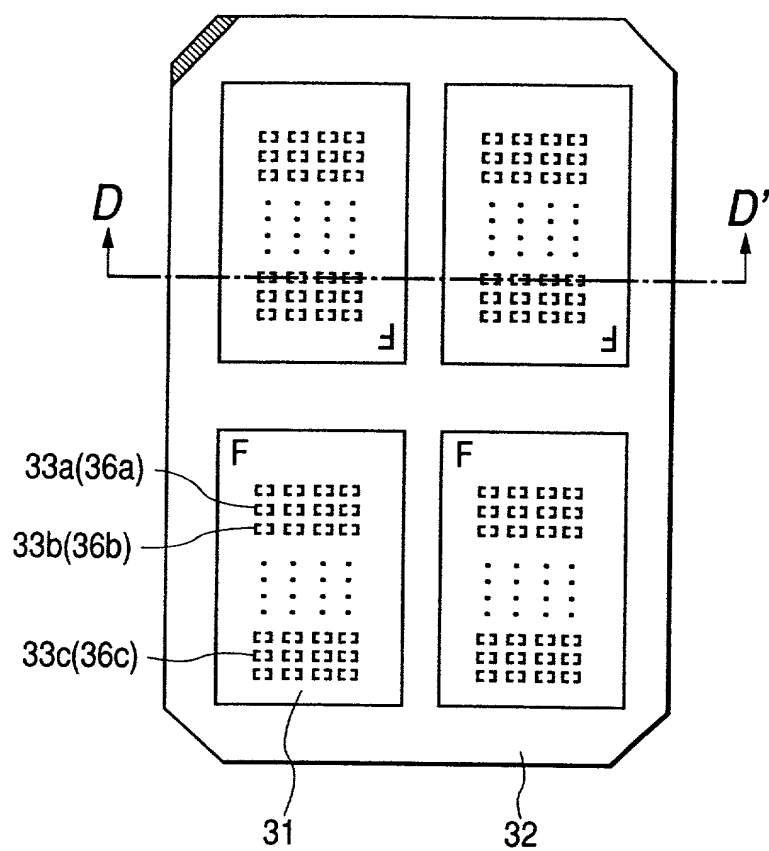


FIG. 31

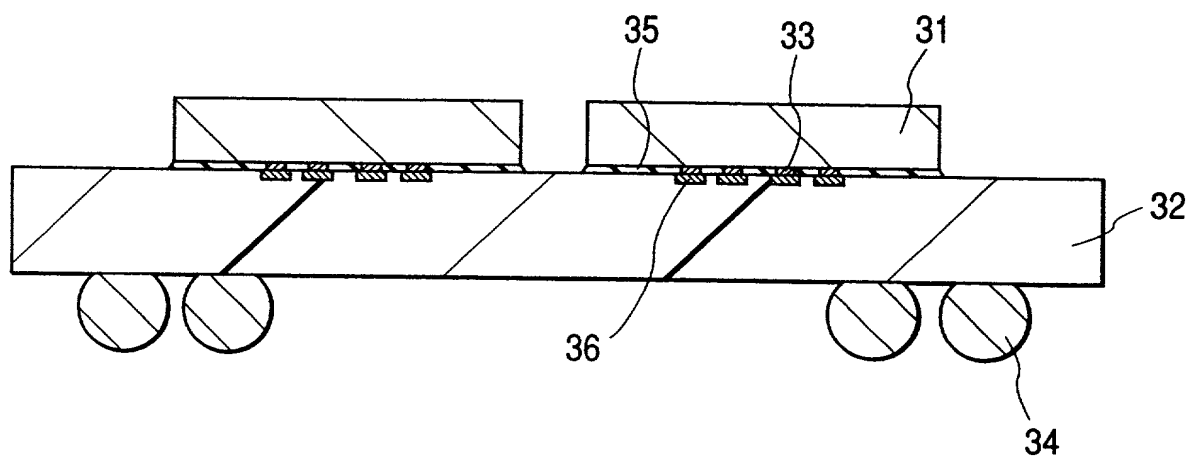


FIG. 32

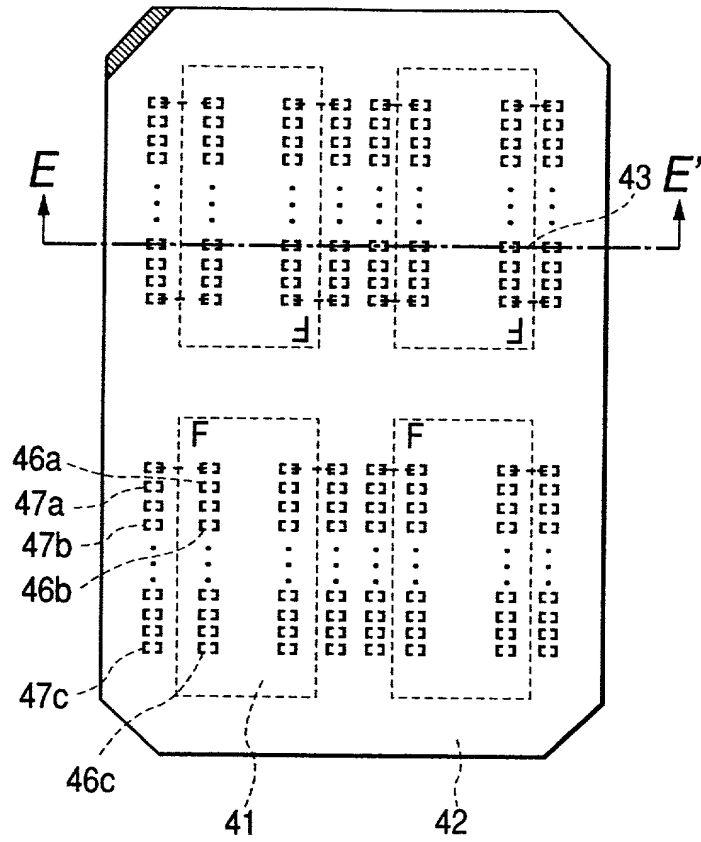


FIG. 33

